IBM

B: Remarks:

The rejection of Claim 1 upon which all the claims are dependent is in view of:

- Watai (US Patent No. 5,745,373) which teaches how to reduce gates on logical circuits using programming tree structures along with a library of circuits and properties. The original design is read in, mapped to the tree structure, and then optimized using their technique. Watai does not provide an orthogonality checker nor a hierarchical structure.
- Meaney (US Patent No. 5,996,040) which teaches a hierarchical structure of scalable muxes that have built-in orthogonality checkers, ORs, and muxes which can be reconfigured without changing the control strucures. It also teaches that orthogonality checkers can be built hierarchically, but Meaney the reference does not teach how to optomize an hierarchical orthogonality structure for said hierarchical design of said circuit while maintaining a hierarchical design for a circuit.

Neither referenced patent teaches how to OPTIMIZE the hierarchical orthogonality structure itself, and claim 1 has been modified to move the preamble down into the claim itself and to add "and to optomize the hierarchical orthogonality structure." The applicants find not teaching and do not believe that, if the Watai method could be adapted to achive the end, Watai's method would even converge on the solution proposed and claimed. One thing is certain there, however. Watai always works on a FLAT design. They do not teach how to maintain hierarchies throughout a design. Further, they do not teach how to CHANGE the hierarchy levels to optimize, while keeping a hierarchical design. The

applicants do not use Watai, so how Watai could teach applicant's claimed method is not something that one of ordinary skill in the art would undertake, let alone use to accomplish the claimed subject matter. The applicants do not use programming trees to represent the input/outputs or their polarities, not even manually.

For instance, if we have a 9-way MUX built as three 3-way muxes, the applicants would also build the 3-way orthogonality checkers with the muxes. Watai would optimize the muxes one way and but how he would build the checkers is not apparent. Would he implement possibly the orthogonality checkers independently?

Meaney on the other hand in the reference cited teaches how to implement a hierarchical orthogonality checker GIVEN a hierarchical MUX structure. However, if the applicants here wanted to optimize the orthogonality portion of that, Meaney (an inventor here) does not teach in the earlier reference how to trade-off these hierarchical levels.

For instance, one could speculate that Meaney may have built a 3+3 MUX/ORTH or a 2+2+2 MUX/ORTH to accomplish a 6-way hierarchical MUX with orthogonality. Which is optimum? Meaney the reference does not teach that. Even if one optimizes the 3+3 or the 2+2+2 at each stage, which is choosen? Are there other combinations? Neither Meaney nor Watai nor any combinarion of the two teach any of these considerations or even mention this specific problem as something to solve. Nor do they teach in combination any element of the dependent claims, which are separately patentable.

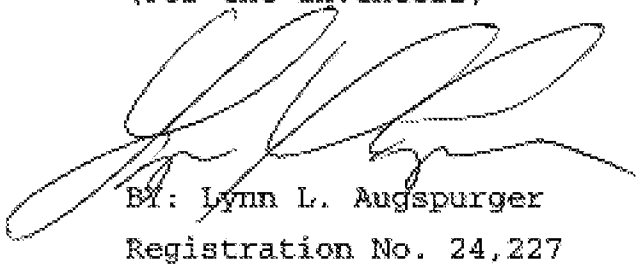
This invention when implemented allows one determine whether to build 2+4, 3+3, or 2+2+2 hierarchical orthogonality checkers or

even a 6-way flat one, based on the library available to optimize area and gate counts. That would not be acheived by the references combined by the examiner.

Any futher changes in language that the examiner believe appropriate can be agreed to by telephone if required.

It is respectfully submitted that the application should be in final condition for allowance which is respectfully requested.

RESPECTFULLY SUBMITTED
(For the inventors)



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